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Ph.D. Public Defense

Friday, October 10, 2014
9:00 AM
Computer Studies Building 426

Energy-Efficient, High-Speed Integrated Circuits for Emerging Computing and Sensing Applications

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Abstract

Today, high-speed integrated circuits (ICs) are advancing rapidly, driven by the ever-increasing demands for larger bandwidth and better energy efficiency in high performance computing and communications. This is evident in several research areas involving the most critical components in these applications such as on-chip clocking and interconnect. In addition, high-speed ICs are enabling emerging sensing applications, for Internet of Things such as short-distance radars.

In recent years, high-speed ICs have gradually migrated from III-V technologies to silicon-based technologies, driven by the latter's rapid advances in device performance, significant cost advantage, and system-on-a-chip (SoC) capability. However, designing silicon-based high-speed ICs still faces many challenges, such as significant parasitics effects and large signal attenuation due to the lossy silicon substrate. Moreover, high energy efficiency becomes increasingly important, especially in mobile and densely populated devices.

In this thesis, I will address these challenges in three different high-speed circuits and systems targeting emerging computing and sensing applications, namely,
a) injection-locking frequency multiplier (ILFM), b) a new on-chip transmission-line based interconnect system, and c) an integrated light detection and ranging (LIDAR) system.

Recently, the injection locking circuit technique is increasingly used in high-speed clock generation and distribution, thanks to its advantages in high operation fre- quency and low power consumption. In this work, a new ILFM is proposed and designed for on-chip clock distribution applications. It uses multiphase injection and built-in harmonic generation to increase locking range and reduce power consumption. Two multiply-by-2 ILFM prototypes are implemented in 130-nm CMOS technology, and achieve wide locking range up to 116%, low power consumption, and compact chip area.

The global interconnects for data communications in a multi-core chip becomes increasingly critical. Compared to network-on-chip approach, the proposed transmission- line based interconnect system exhibits significant advantages in bandwidth, circuit complexity, latency, and energy efficiency. As part of a collaborative project, energy- efficient high-speed circuits are designed for this interconnect system. The prototype is implemented in 130-nm BiCMOS technology, and achieves date rate up to 25.4
Gb/s with energy efficiency 1.67 J/b.

LIDARs are increasingly adopted in smart sensor systems. In this work, a LIDAR system is proposed for emerging medical sensing applications. Based on pulsed time-of-flight principle, the LIDAR system integrates an optical transceiver and optical devices. My work focuses on energy-efficient high-speed LIDAR transceiver design. The fully integrated transceiver prototype is designed in 130-nm BiCMOS technology, and has measurement range 0.5-10 m, accuracy less than 130 ps, and power consumption 39.5 mW.

In summary, by new circuit techniques and careful design, silicon-based ICs can achieve high-speed and good energy efficiency for emerging computing and sensing applications.